ABSTRACT OF THE DISCLOSURE

An adder 11 outputs a signal VS indicating a value of (Vr-Vo), and a multiplier 12 outputs a control signal GS indicating a value of G(Vr-Vo) on the basis of the signal VS. An adder 13 outputs a signal HS on the basis of the control signal GS and a signal FS outputted from an operation circuit 30, and a PWM signal generating circuit 20 generates a PWM signal KS on the basis of the signal HS and a ramp signal RS outputted from a ramp signal circuit 15, and outputs this signal KS to a switching power supply. A counter 14 counts an on time of the PWM signal KS and retains a count value at a time of receiving a sample signal SMP. The operation circuit 30 has a high-pass filter 31 and an integrator 32, performs an operation based on a signal DS indicating the count value outputted from the counter 14, and outputs the signal FS after the operation.